CLAIMS

1. A method of making an integrated circuit, comprising:

defining a model of a circuit for use on the integrated circuit;

generating circuit equations of the model;

determining a steady state response of the model to large signal excitations;

linearizing about the steady state response to obtain a first order transfer function;

determining a first order response of the model;

determining a second order response of the model using the first order transfer function and the first order response;

determining a third order response of the model using the first order transfer function and the second order response;

analyzing results of the third order response to determine if the circuit is ready to be manufactured; and

manufacturing the integrated circuit.

2. The method of claim 1, wherein the circuit is an analog circuit.

3. The method of claim 1, wherein the circuit equations are formulated in the time domain.

4. The method of claim 1, wherein the circuit equations are formulated in the frequency domain.

5. The method of claim 1, wherein the circuit equations are formulated as being time-invariant.

6. The method of claim 1, further comprising:

modifying the circuit design after the step of analyzing and before the step of manufacturing.

7. A method of analyzing a circuit, comprising:

generating circuit equations of a model of the circuit;

deriving a first order transfer function of the model;

determining a first order response of the model using the first order transfer function; and

determining a second order response of the model using the first order transfer function and the first order response.

8. The method of claim 7, further comprising:

determining a third order response of the model using the first order transfer function and the second order response.

9. The method of claim 8, further determining a steady state response to large signal excitations of the model, and wherein the step of determining a first order response further comprises using the steady state response.

10. Using the method of claim 9 to identify shortcomings of the circuit, then modifying the circuit to overcome the shortcomings and manufacturing the circuit as modified.

11. A method of estimating a first solution of a circuit based on first predetermined inputs to the circuit, comprising:

determining a system of equations representing a general solution of the circuit;

determining a second solution of the circuit based on the general solution at second predetermined inputs;

determining a first order transfer function of the general solution at the second predetermined inputs;

solving for a first order estimate of the first solution using the first order transfer function at the second predetermined inputs and the second solution; and

solving for a second order estimate of the first solution using the first order transfer function at the second predetermined inputs and the first order estimate.

12. The method of claim 11, further comprising:

solving for a third order estimate of the first solution using the first order transfer function at the second predetermined inputs and the second order estimate.

13. The method of claim 12, wherein the first solution comprises voltages at nodes within the circuit.

14. The method of claim 11, wherein the equations comprise time domain equations.

15. The method of claim 11, wherein the equations comprise at least one of frequency domain equations and time domain equations.

16. The method of claim 11, wherein the equations comprise time-invariant equations.

17. Using the method of claim 11 to identify shortcomings of the circuit, then modifying the circuit to overcome the shortcomings and manufacturing the circuit as modified.

18. The method of claim 17, wherein the first solution comprises voltages at nodes within the circuit, further comprising:

identifying a contribution of each node to a total distortion of the circuit.

19. The method of claim 11, wherein the equations are Kirchoffs laws, and wherein the step of solving for the second order estimate comprises solving a first mathematical formula comprising the first order estimate and a first mathematical expression using the first order transfer function at the second predetermined inputs multiplied by the difference between the first order estimate and the second order estimate.

20. The method of claim 19, further comprising:

solving for a third order estimate of the first solution using the first order transfer function at the second predetermined inputs and the second order estimate.

21. The method of claim 11, wherein the step of solving for the third order estimate comprises solving a second mathematical formula comprising the second order estimate and a second mathematical expression using the first order transfer function at the second predetermined inputs multiplied by the difference between the second order estimate and the third order estimate:

22. A computer-readable medium having stored instructions for directing the operation of a computing device, wherein the stored instructions are for directing the computing device to:

generate circuit equations of a model of the circuit;

derive a first order transfer function of the model;

determine a first order response of the model using the first order transfer function; and

determine a second order response of the model using the first order transfer function and the first order response.

23. The computer-readable medium of claim 22 wherein the stored instructions are for further directing the computing device to:

determine a third order response of the model using the first order transfer function and the second order response.